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Piezoresistive silicon nanowire resonators as embedded building blocks in thick SOI

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Abstract

The use of silicon nanowire resonators in nanoelectromechanical systems for new-generation sensing and communication devices faces integration challenges with higher-order structures. Monolithic and deterministic integration of such nanowires with the surrounding microscale architecture within the same thick crystal is a critical aspect for the improvement of throughput, reliability and device functionality. A monolithic and IC-compatible technology based on a tuned combination of etching and protection processes was recently introduced yielding silicon nanowires within a 10 μm-thick device layer. Motivated by its success, the implications of the technology regarding the electromechanical resonance are studied within a particular setting, where the resonator is co-fabricated with all terminals and tuning electrodes. Frequency response is measured via piezoresistive readout with frequency down-mixing. Measurements indicate mechanical resonance with frequencies as high as 100 MHz exhibiting a Lorentzian behavior with proper transition to nonlinearity, while Allan deviation on the order of 3–8 ppm is achieved. Enabling the fabrication of silicon nanowires in thick silicon crystals using conventional semiconductor manufacturing, the present study thus demonstrates an alternative pathway to bottom-up and thin silicon-on-insulator approaches for silicon nanowire resonators.

Keywords: silicon nanowire, nanowire resonator, piezoresistive readout, top-down fabrication, semiconductor manufacturing, NEMS

(Some figures may appear in colour only in the online journal)

1. Introduction

Integrated circuits (ICs) have witnessed a unique improvement in functionality and performance through downscaling, while significant challenges lie ahead for keeping up the pace of miniaturization [1]. Semiconductor manufacturing is marching toward three-dimensional (3D) ICs to overcome complexity of miniaturization in conventional planar devices [2], where batch fabrication of multiple length scales is the immediate challenge. A similar development is taking place in micro electromechanical systems (MEMS), where new-generation physical sensors exploit the mechanical sensitivity brought by the introduction of piezoresistive silicon nanowire (Si NW) gages into conventional MEMS architecture [3, 4]. With a two-order-of-magnitude difference between the MEMS layer thickness and the critical dimension (CD) of the Si NW, the associated setting is inherently 3D. In addition to their role as stress concentration elements leading to elevated mechanical sensitivity in MEMS, Si NWs have further significant advantages such as overcoming signal losses and increasing resonance frequency, two features already widely used in nano electromechanical systems (NEMS). Si NWs obtained via bottom-up techniques provide a high mechanical quality factor, Q, and are also reported to exhibit

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giant piezoresistivity [5, 6], a feature specifically suited for electromechanical resonator applications. Although studies of the resonance behavior of such bottom-up Si NWs [7] report high-frequency operation along with on-chip actuation and detection capabilities [8], an implementation of the array configuration, for example for sensing applications [9], remains challenging due to the inherent limitations of the bottom-up technique regarding alignment and registration [10].

Alternatively, Si NW resonators on CMOS platforms are obtained by the top-down approach [11, 12] offering low-power consumption and scalable transduction [13]. Top-down technologies are mainly available for thin microelectronic substrates, where the out-of-plane dimensions of the Si NW resonator and the surrounding architecture are the same [14–16]. For the cases where the Si NW has to be attached to a much thicker MEMS device, a similar approach is adopted, where the nanoscale component is fabricated in thin silicon on insulator (SOI) first. This is then followed by the deposition of a 10 μm-thick structural Si layer dedicated to MEMS fabrication [4]. This multiscale technique is shown to work well in applications such as 3D inertial sensors [4], magnetometers [17] and gyroscopes [18].

Si NWs can also be obtained within the same thick Si crystal as the rest of microscale device. For example, Si NWs can be obtained in bulk Si through using an oxide encapsulation around a nanoscale protrusion followed by a plasma etching process for release [19]. An alternative approach employs Ga^+ doping by focused ion beam (FIB) imparting etch selectivity to the doped region. A subsequent etching process releases Si NWs attached to microscale terminals [20, 21]. A more recent study reports the co-fabrication of Si NWs with MEMS by tuning the involved deep etch (DRIE) process such that fine scallops define a nanoscale beam, while subsequent coarse scallops release it and simultaneously generate MEMS [22].

Although top-down techniques based on semiconductor manufacturing provide the most promising pathway for on-chip integration with parallel processing capability and dimensional control [23], the following disadvantages associated with the aforementioned technologies remain:

(i) In the early example of oxide protection, intensive etch rate in the protective layer limits the etch depth to a very shallow trench. Therefore, the challenges of preserving Si NWs in plasma etching impose thickness uniformity issues via RIE [19]. Although isotropic release is reported recently with sidewall passivation through C_4H_8 as well, a similar difficulty to retain the Si NW in plasma etching confines the ultimate etch depth for a minimum Si NW thickness. An ultimate trench depth of 3 μm for a released Si NW with a CD of about 500 nm is reported [24].

(ii) A more recent example employs a much thicker initial protrusion instead of sidewall passivation defined in etch cycles with fine scallops. This is then followed by etching with coarse scallops for an isotropic release. While a subsequent oxide thinning reduces the sidewall roughness and the Si NW cross-section, preserving sub-micron trench width—specially in MEMS devices—and inducing residual stresses at high temperatures are the major drawbacks. This technique yields a Si NW with CD of 100 nm on a 5 μm-thick device layer [22].

(iii) In FIB-induced Ga doping , the depth of ion implantation limits the NW thickness in addition to the loss of single-crystal nature of the doped region [20, 21]. A recent study shows the help of annealing on the recovery to crystallinity [25]. A suspended Si NW with a CD of 20 nm between microscale structures with 2 μm trench depth is reported by this approach [21].

To address these challenges a monolithic technology for incorporating Si NWs in thick SOI wafers was introduced recently, where the Si NW remains an integral part of the SOI device layer, in which other components such as MEMS are co-fabricated [26–29]. This is achieved through a combination of high-resolution lithography and a two-step etching process. The first shallow etch creates a nanoscale protrusion on the surface, which is then released through the isotropic etch component of the following DRIE. Although this final etch depth is very large compared to the CD of the Si NW, protective layers around the Si NW in addition to the appropriate DRIE recipe proved to work well. Si NWs are not attacked along their unprotected bottom surface. In the first demonstration, the technique delivers Si NWs with a CD of 35-nm spanning at least 10 μm-deep trenches [28]. Recently, this monolithic technology is improved for the integration of Si NWs with microscale architectures with an extreme trench depth of 40 μm [26].

Although the applicability of this new technology to the piezoresistive measurement of small forces was also recently demonstrated utilizing MEMS [3], it was realized only under quasistatic conditions. The present study is the first report of the resonance behavior of such piezoresistive Si NWs obtained in thick SOI substrates. Electrostatic actuation and piezoresistive readout are utilized. Resonance behavior is characterized for a NW geometry embedded within a 10 μm-thick device layer. In the remainder of the paper, architecture and preparation of suspended Si NWs between microscale ports are introduced first. The device is intended to operate as a mechanical resonator with piezoresisive transduction. Frequency response for first and second modes is analyzed using frequency down-mixing technique. The electromechanical characterization is followed by studying nonlinearity and frequency stability. The work is concluded by introducing the applications of the technique for new-generation sensors and power-efficient ICs through addressing the shortcomings associated with available bottom-up and thin-SOI technologies.

2. Device architecture and sample preparation

The device is designed based on a suspended piezoresistive Si NW electromechanical resonator spanned between microscale electrodes. One lateral gate induces a mechanical vibration in the double-clamped Si NW. The piezoresistive behavior of the highly-doped Si NW provides the transduction between mechanical and electrical domains. Fabrication technique is developed on a 100 mm-diameter, highly doped $\langle 1\,0\,0 \rangle$ SOI wafer with a 10 μm-thick device layer, a 1 μm-thick

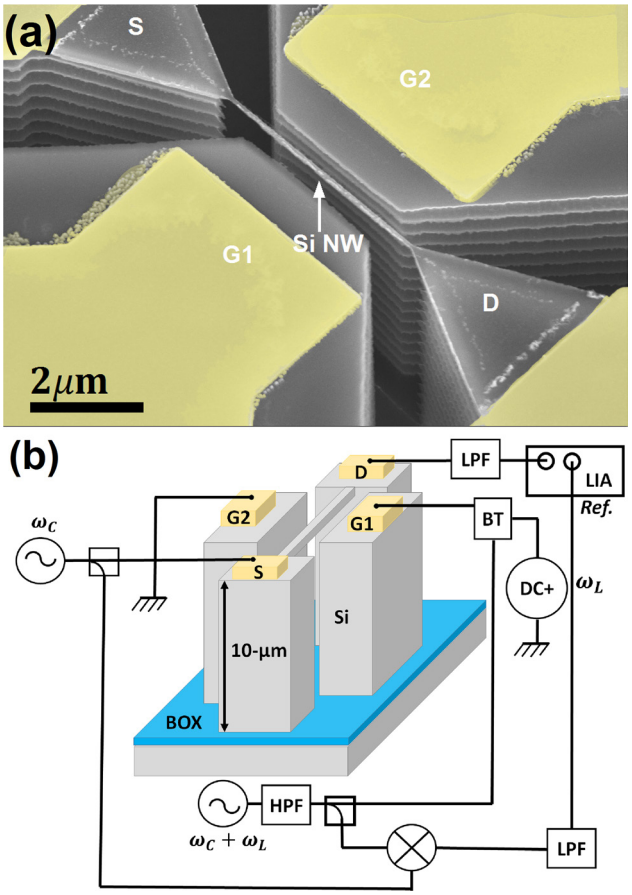

Figure 1. (a) Si NW resonator along ⟨1 0 0⟩ with a 5 μm length, 100 nm width and 200 nm thickness surrounded by two electrostatic gates with a gap of 400 nm. False color in yellow represent metal pads. (b) Schematic diagram of the measurement circuit. LIA: lock-in amplifier, BT: bias tee, LPF: low-pass filter, HPF: high-pass filter.

buried oxide (BOX), and a 380 μm-thick handle layer. The wafer is doped with phosphorous to a mean resistivity of $5 \times 10^{-4}\ \Omega \cdot \mathrm{cm}$. A high-resolution lithography defines the Si NW width, while the subsequent reactive ion etching (RIE) process sets the Si NW thickness. Fabrication details can be found elsewhere [26, 28, 29]. It should be emphasized that this technique yields Si NWs on the top surface of the SOI device layer, in which other microscale features are generated in the same batch by preserving an up to two-order-of-magnitude scale difference. This scale-up integration has been possible thanks to a combination of different etching steps while protecting the rather fragile Si NW.

One such Si NW between two lateral electrodes is shown in figure 1(a). A gap of 400 nm between the Si NW and electrodes is achieved corresponding to a trench aspect (depth-to-width) ratio of 25. Frequency response of the device is characterized based on the frequency down-mixing approach. The high-frequency signal from the mechanical motion, ω_c, of the resonator is converted to a lower frequency, ω_L, to be detected by a lock-in amplifier. The frequency response is measured based on the two source-1ω detection mechanism, having resistance changes proportional to the Si NW deflection [30]. In this technique, Si NW is at excitation frequency, $V_{\mathrm{NW},1\omega} = V_{\mathrm{NW}}^{\mathrm{AC}} \cos(\omega_c)$,while the gate has a small offset,

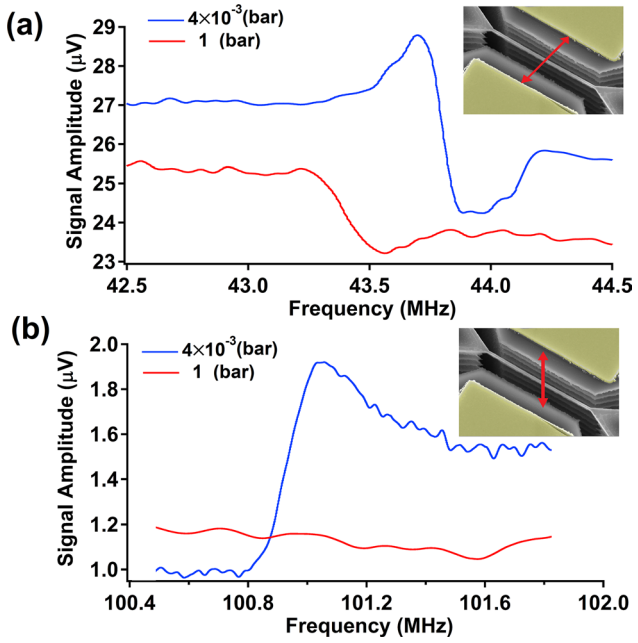

Figure 2. (a) First-mode frequency response of the device at drive NW voltage $V_{\mathrm{NW}}^{\mathrm{AC}} = 0.4$ V and driving bias voltage $V_{\mathrm{gate}}^{\mathrm{AC}} = 6$ V at a DC level of $V_{\mathrm{gate}}^{\mathrm{DC}} = 6$ V at the atmospheric pressure and a pressure of 4×10^{-3} bar, (b) Second-mode frequency response of the device at drive NW voltage $V_{\mathrm{NW}}^{\mathrm{AC}} = 0.4$ V and driving bias voltage $V_{\mathrm{gate}}^{\mathrm{AC}} = 10$ V at a DC level of $V_{\mathrm{gate}}^{\mathrm{DC}} = 15$ V at the atmospheric pressure and a pressure of 4×10^{-3} bar. (All AC voltages are expressed in terms of the peak-to-peak magnitude).

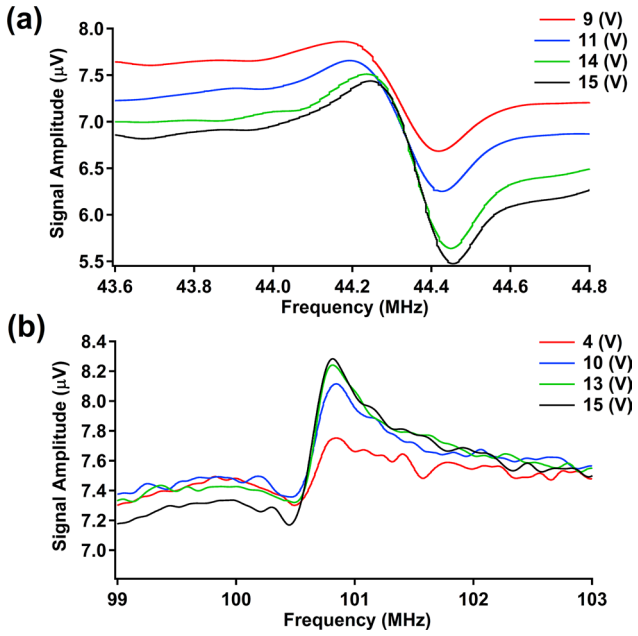

Figure 3. (a) First-mode, and (b) Second-mode electromechanical resonance for various bias voltages, $V_{\mathrm{gate}}^{\mathrm{DC}}$, at a drive voltage of $V_{\mathrm{NW}}^{\mathrm{AC}} = 0.4$ V and a driving bias voltage of $V_{\mathrm{gate}}^{\mathrm{AC}} = 6$ V measured at a pressure of 4×10^{-3} bar and room temperature. (All AC voltages are expressed in terms of the peak-to-peak magnitude).

$V_{\mathrm{gate},1\omega} = V_{\mathrm{gate}}^{\mathrm{AC}} \cos(\omega_c + \omega_L)$, (figure 1(b)). Measurement is carried out at different pressure levels to verify the mechanical nature of the resonance, further facilitating an appropriate

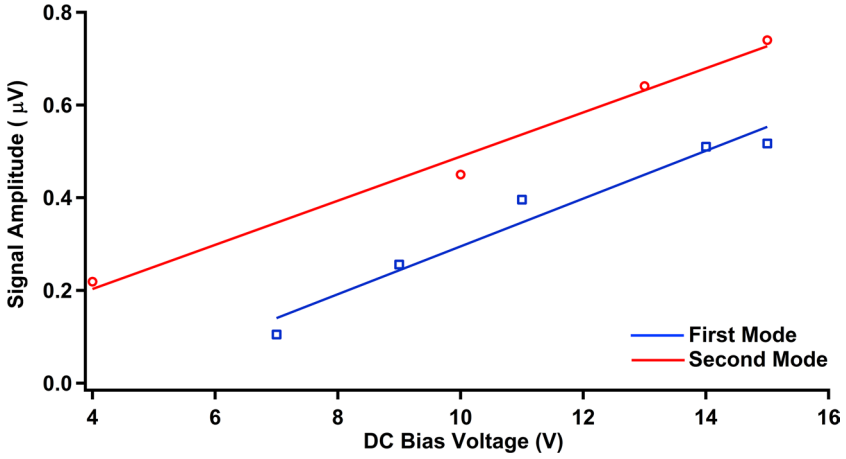

Figure 4. The linear variation of the signal amplitude with DC bias voltage, $V_{\text{gate}}^{\text{DC}}$.

comparison with the literature. A vacuum chamber is used, where one can work at the minimum pressure level smaller than 10^{-9} bar. Furthermore, the temperature of the sample holder can be decreased to 100 K. Dice with Si NW resonators are wire-bonded to PCB for further electrical connections.

3. Results and discussion

Measurements are first taken at two different pressure levels of 1 bar and 4×10^{-3} bar. Frequency sweeps around the first and second modes of the Si NW are shown in figures 2(a) and (b), respectively. Curve fitting is carried out based on the Lorentzian function. The resonance peak is detected at 43.69 MHz for the first mode and 101.03 MHz for the second mode. Q values of approximatley 100 and 250 are obtained for the first mode at the atmospheric pressure and in vacuum, respectively. Q obtained at the atmospheric pressure is comparable to those reported for other top-down Si NWs on thin SOI [31]. The increase of Q obtained through the reduction of the pressure verifies the mechanical nature of the signal. Considering the oxide encapsulation around the Si NW with a trapezoidal cross-section [26, 28, 29], a finite element analysis for the frequency response of the resonator architecture yields a resonance frequency of 47.09 MHz and 100.98 MHz for the first and second modes, respectively. Vibration directions are also indicated by arrows in the insets in figure 2.

Frequency response for different gate bias voltages, $V_{\text{gate}}^{\text{DC}}$, is obtained through sweeping $V_{\text{gate}}^{\text{DC}}$. Results are depicted in figure 3. For the first mode, increasing the bias voltage from 9 V to 15 V changes the signal amplitude from 0.25 μV to 0.51 μV improving Q from 290 to 340 at the pressure of 4×10^{-3} bar (figure 3(a)). Second-mode peaks for the same device can be seen in figure 3(b). An increase in signal amplitude from 0.21 μV to 0.74 μV is observed by sweeping $V_{\text{gate}}^{\text{DC}}$ from 4 V to 15 V changing Q from 280 to 330. While Q values are comparable to those of some of the Si NW resonators obtained on thin substrates [25, 32], it also exhibits deviations, sometimes up to one order of magnitude, with the rest of the top-down [11–13, 19] and bottom-up [8, 30] technologies. At this point it is important to note that the measurement pressure is considerably higher compared to high-vacuum conditions. Finally, a linear dependence of the signal amplitude on the bias voltage is observed for both modes as depicted in figure 4. This observation is a sign of the Lorentzian nature of the mechanical resonance, as the linear piezoresistive transduction in 1ω-detection technique yields a resistance change proportional to the Si NW deformation [8, 33].

Furthermore, a nonlinear transition in the first mode is achieved by increasing $V_{\text{gate}}^{\text{DC}}$ up to 10 V at a sample holder temperature of 100 K and pressure $<1 \times 10^{-9}$ bar (figure 5). Increasing bias voltage from 3 V to 10 V changes the signal amplitude from 2 μV to 8.4 μV with a shift in the resonance frequency from 45.43 MHz to 45.65 MHz. This transition changes Q from 700 to more than 1000. A nonlinear behavior in Si NW resonator with mechanical hardening similar to those reported on thin SOI [34] is achieved providing a large dynamic motion for high-resolution sensing and signal processing applications. The nonlinearity can be characterized through using the critical response amplitude [34]. The solid red line shows the fitting peaks of resonant curves based on the obtained resonance frequency and Q in linear regime. The Lorentzian fits in linear vibration are demonstrated as dashed lines in the inset to figure 5. Further studies on the role of the readout scheme involving down-mixing in addition to the semiconductor nature of the resonator can shed light on the deviation present in the background fit. We also note that the field effect arising from the electrostatic actuation could modulate the resistance, while this effect for the highly-doped Si NW of this work is negligible [3, 26]. Hence, the modulated resistance in the Si NW is a direct result of the mechanical strain induced during resonance.

Frequency stability (Allan deviation) measurement is carried out as well for the first-mode (figure 6). A fractional frequency fluctuation on the order of 3–8 ppm is achieved. As a mass sensor this resonator with an effective mass in the order of $M_{\text{eff}} \approx 170$ fg would offer a mass resolution of $\delta M \approx 1.0$ ag. The Allan deviation obtained in this study is comparable to those reported by previous top-down techniques for high-resolution detection [11, 12]. This stability can be improved through further size reduction in cross-section and surface improvement of Si NWs for achieving higher Q [35].

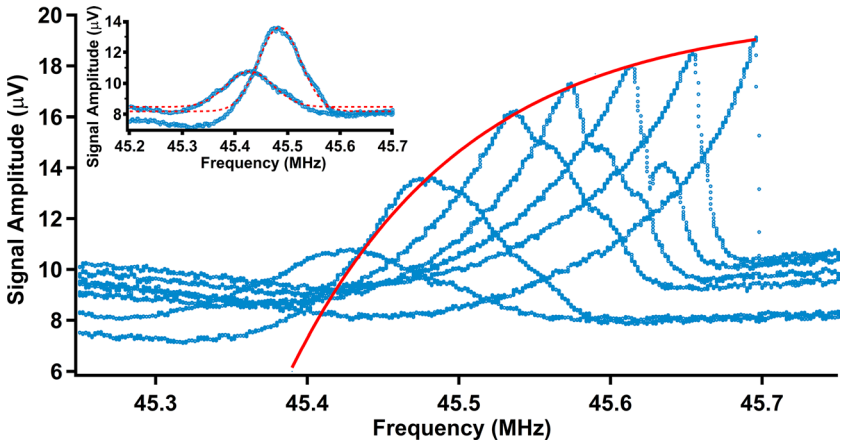

Figure 5. Linear to nonlinear transition in the first mode for a series of bias voltages, $V_{\text{gate}}^{\text{DC}}$, between 3 V to 10 V at a drive voltage of $V_{\text{NW}}^{\text{AC}} = 0.4$ V and a driving bias voltage of $V_{\text{gate}}^{\text{AC}} = 10$ V measured at a pressure of 2×10^{-12} bar and stage temperature of 100 K. (All AC voltages are expressed in terms of the peak-to-peak magnitude). The solid red line indicates the mechanical nonlinearity response. Linear resonance is shown in the inset. The red dashed line in the inset is a Lorentzian fit.

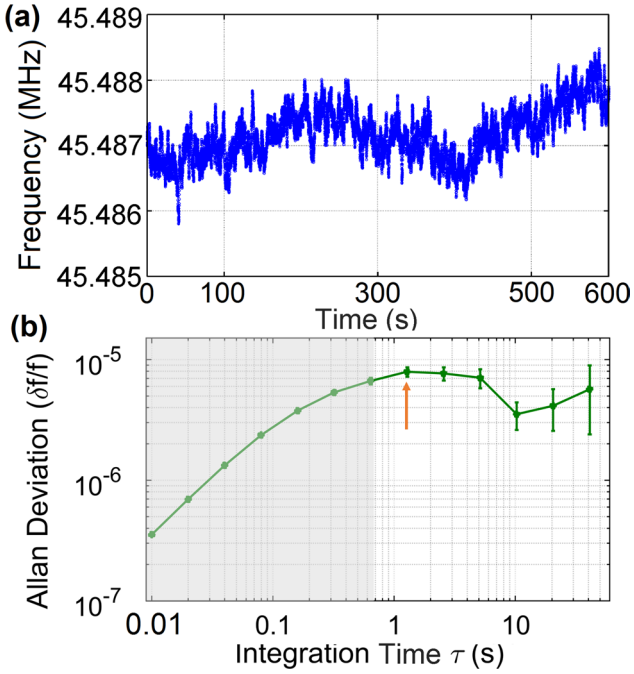

Figure 6. (a) Frequency versus time, (b) Allan deviation as a function of the integration time taken at 100 K stage temperature, under a pressure of 2×10^{-12} bar. With the arrow in (b) indicating the response time of the PLL, values for shorter time scales do not reflect the actual unstability.

The proposed monolithic integration of the Si NW with the surrounding microscale architecture within the same Si crystal eliminates assembly drawbacks related to bottom-up approaches. As discussed earlier in Introduction it also eliminates a series of complications and restrictions associated with available top-down techniques. In this work this point is demonstrated for the case of electromechanical resonators. Based on standard IC-compatible processes, the fabrication technology is shown to deliver Si NW electromechanical resonators within a thick substrate with a two-order-of-magnitude scale difference between the Si NW and the surrounding architecture. Operation frequencies demonstrated are in the order of

Table 1. Features of the Si NW resonator embedded in thick SOI.

Q			f (MHz)		M_{eff} (fg)	δM (ag)	$\delta f/f$ (ppm)
1 (bar)	4×10^{-3} (bar)	$< 1 \times 10^{-9}$ (bar)	First-mode	Second-mode	170	1.0	3–8
98.3	≈300	≈700	43.7	101			

those reported in thin SOI [11–13], trench etching [14, 19, 25] and bottom-up [8, 30] studies. The obtained Q for embedded Si NW resonator in thick SOI is also found to be comparable to those of several top-down reports [25, 31, 32]. This approach provides a frequency stability in a similar range to that reported by thin-SOI work [11, 12]. Furthermore, the presented technology demonstrates the tuning to nonlinearity by electrostatic mechanism similar to available approaches [8, 32, 34] facilitating large dynamic motion in Si NW resonators embedded in thick substrates for new-generation sensing and communication devices. The essential features of the suspended Si NW resonator in thick SOI is summarized in table 1.

The present study addresses the integration of Si NW resonators with higher-order structures in modern electronic devices [17, 36]. Implementation of *in situ* actuation and readout in electromechanical resonators can also enable the incorporation of large resonator arrays in very-large scale integration (VLSI) [9, 11]. Resonance can further be improved through downscaling the Si NW cross-section, controlling doping level for higher piezoresistive gage factors [5, 6] and reducing the surface roughness [35]. The e-beam lithography step imposes a sidewall and line edge roughness that can be reduced through proximity effect correction technique [26]. In the present technology, the size reduction can be carried out by the definition of initial protrusions via lithography and shallow etch steps to decrease the width and the thickness of the Si NW, respectively [3, 28, 29]. A diffusion technique is utilized to dope the Si top surface to a mean resistivity of $5 \times 10^{-4}\ \Omega \cdot \text{cm}$ to prevent any electrical contact issues [3, 26]. However, a higher level of resistivity is required to yield the optimum gage factor [5].

Hence, with appropriate definition of the doping level on the Si NW, one can, in principle, get better gage factors.

4. Conclusion

In this study, the resonance behavior of piezoresistive Si NWs embedded in thick SOI is presented as an implication of the recently introduced monolithic and IC-compatible technology based on a tuned combination of etching and protection processes. The co-fabrication of Si NW electromechanical resonators with surrounding microscale terminals and tuning electrodes is demonstrated on a 10 μm-thick SOI device layer, where a two-order-of-magnitude scale difference is preserved. While a nearby gate is used for electrostatic actuation, the piezoresistivity of the Si NW resonators is utilized for the readout, resulting in an on-chip, 3D resonator architecture. Using frequency down-mixing technique the mechanical nature of resonance with frequencies as high as 100 MHz is verified through both pressure damping and the transition to nonlinearity. The overall operation of suspended Si NW resonators in thick substrate is comparable to those reported through available top-down, including thin SOI and trench etching, technologies. By addressing deficiencies related to the available bottom-up and top-down SOI technologies for delivering similar electromechanical resonators, the present work provides a monolithic technology for new-generation sensors and 3D-ICs in modern electronic devices.

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